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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/405,945	09/27/1999	BO JIN	CY-0006	1072

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EXAMINER
UMEZ ERONINI, LYNETTE T

ART UNIT	PAPER NUMBER
1765	13

DATE MAILED: 10/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Application No.	Applicant(s)
09/405,945	JIN ET AL.
Examiner	**Art Unit**
Lynette T Umez-Eronini	1765

Office Action Summary

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____
4) ☐ Interview Summary (PTO-413) Paper No(s) ____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsue (US 5,378,654) in view of Chang et al. (US 5,893,740).

Hsue teaches in the prior art, a conventional method of forming a self-aligned contact (SAC) (same as applicant's contact hole) on a MOSFET device (column 1, lines 6, 7, 25-27, and Figure 1A-1F). The method comprises:

forming silicon dioxide **21** (insulating layer) over polysilicon gate structures **15** (transistor gate) and substrate **10** (Figure 1A), forming silicon oxide spacers **18** (insulating sidewalls) on the polysilicon gate structures **15** (Figures 1C-1F), forming a SAC opening in the silicon oxide layer **21**, and etching a portion of the silicon dioxide layer **21** that is exposed through a mask **22** to open a portion of the surface of N+ doped region (column 2, lines 14-19 and Figures **1E** and **1F**). The above method lacks an etch stop layer over the insulating layer (silicon dioxide **21)**, which reads on,

forming a contact hole through a first insulating layer that is self-aligned with respect to a transistor gate without forming a contact hole etch stop liner.

Hsue differs in failing to teach a transistor having a gate length of less than 0.2 microns.

Chang forms a gate electrode of 0.1 μm and less in length (column 4, lines 10-32, 55 and 56) and a source/drain region (column 4, lines 42-45). Hence, the combination of Chang's gate electrode and source/drain region forms a transistor gate having a gate length less than 0.2 microns as claimed in the present invention. Chang further teaches, higher drive capability and lower parasitic junction capacitance increases switch speed, which is an advantage of having a gate length of less 0.1-micron (column 4, lines 55-64).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hsue by using a transistor with a gate length of less than 0.2 microns as taught by Chang for the purpose of increasing the switching speed.

3. Claims 2 and 4-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsue ('654) in view of Chang ('740) as applied to claim 1 above, and further in view of Nulty et al. (5,468,342).

Hsue differs in failing to teach etching through a first insulating layer comprising non-densified doped silicon dioxide, in claim 2.

Nulty teaches forming contact openings in an oxide layer (column 4, lines 21 and 22). The oxide layer may be undoped or doped, for example BPSG (borophosphosilicate glass) (column 1, lines 17-25) by reactive ion etching (column 1, lines 14-25 and column 6, lines 15-20 and 54-57, and column 7, lines

4-6 and 17-19). The BPSG layer is deposited by CVD (column 6, lines 12-15), which suggests it is a non-densified doped silicon dioxide layer.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hsue in view of Chang by forming a contact hole that includes reactive plasma etching through a first insulating layer comprising non-densified doped silicon dioxide as taught by Nulty for the purpose of isolating regions and layers on a semiconductor device (see Nulty, column 1, lines 13-15).

Hsue in view of Chang differs in failing to specify processing parameters as recited **in claims 4-11**.

Nulty teaches, "various etch parameters such as the gas mixture, temperature, RF power, pressure, and gas flow rate, among others, may be varied to achieve the desired etch characteristics (such as, etch rate, wall slope, anisotropy, etc,) . . ." (column 1, lines 53-55), which suggests that these etch parameters are variable and varying them would result in changing the etch characteristics.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hsue in view of Chang by varying the processing parameters as taught by Nulty for the purpose of obtaining a desired etch characteristic.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsue ('654) in view of Chang ('740) as applied to claim 1 above, and further in Figura et al. (US 5,661,064).

Hsue in view of Chang and further in view of Nulty differs in failing to teach silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

Figura teaches a silicon dioxide material, such as borophosphosilicate glass (BPSG) having phosphorus dopant of from 1 and 10% (column 3, lines 15-18), which falls within the range of phosphorous dopant that is greater than 5%.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hsu in view of Chan by implanting silicon dioxide with a phosphorous dopant that is greater that 5% for the purpose of enhancing the conductive properties of an intrinsic insulative material such as SiO_2.

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsue ('654) in view of Nulty ('342).

Hsue teaches a conventional method of forming a self-aligned contact (SAC) (same as applicant's contact hole) on a MOSFET device (column 1, lines 6, 7, 25-27, and Figure 1A-1F). The method comprises:

etching a contact hole, through a first insulating layer comprising silicon dioxide that is self-aligned with respect to a conductive structure that is formed

over a substrate and includes insulating sidewall (column 2, lines 14-19 and Figures **1A, and 1C-1F**).

Since Hsue etches and uses the same method of etching a contact hole through a first insulating layer that is self-aligned with respect to a conductive structure that is formed over a substrate and that includes insulating sidewalls, as that of the claimed invention, then using Hsue's method would inherently result in an etch selectivity between the first insulating layer and the sidewall that is greater than ten to one, and an etch selectivity between the first insulating layer and the substrate that is greater than one hundred to one.

Hsue differs in failing to teach etching a first insulating layer comprising doped silicon dioxide, **in claim 12**.

Nulty teaches an opening is formed through the BPSG layer by carrying out the etching in a reactive ion etching system (column 1, lines 14-25; column 4, lines 21-22; column 6, lines 15-20 and 54-57; and column 7, lines 4-6 and 17-19), which reads on, etching a first insulating layer comprising doped silicon dioxide.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hsue by forming a contact hole that includes reactive plasma etching through a first insulating layer comprising a doped silicon dioxide as taught by Nulty for the purpose of isolating conductive regions and layers on a semiconductor substrate (see Nulty, column 1, lines 12-15).

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsue ('654) in view of Nulty ('342) as applied to claim 12 above, and further in view of Chang ('740).

Hsue in view of Nulty differs in failing to teach insulating sidewalls comprises silicon nitride.

Chang teaches depositing a layer of dielectric material such as . . . silicon dioxide, silicon nitride combination thereof, and the like is formed and etching the dielectric layer to form sidewall spacers (column 4, lines 33-41).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hsue in view of Nulty by using Chang's method of forming insulating sidewalls comprising silicon nitride because the dielectric materials are seen as equivalent they both form sidewall spacers. Substitution of one for the other would have been obvious for the purpose of improving the method of making a semiconductor device.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsue ('654) in view of Nulty ('342) as applied to claim 12 above, and further in view and Figura ('064).

Hsue in view of Nulty differs in failing to teach silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

Figura teaches a silicon dioxide material, such as borophosphosilicate glass (BSPG) having a phosphorus dopant from 1 and 10%, which falls within the range of phosphorous dopant that is greater than 5% (column 3, lines 15-18).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hsu in view of Nulty by implanting silicon dioxide with a phosphorous dopant that is greater that 5% for the purpose of enhancing the conductive properties of an intrinsic insulative material such as SiO_2

8. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsue ('654) in view of Nulty ('342) as applied to claim 12 above, and further in view and NIPPON STEEL CORP. (English Abstract of JP 100223897, Derwent Information Ltd.) and further in view of Plossl et al. (US 5,907,771).

Hsue in view of Nulty differs in failing to teach forming a hard etch mask comprising an insulating material over the first insulating layer; and forming the contact hole includes etching through the first insulating layer with a selectivity between the first insulating layer and the hard etch mask that is greater than fifty to one, **in claim 16**.

Atsushi teaches forming a hard etch mask comprising an insulating material over the first insulating layer (Abstract). Since Atsushi uses the same method in etching the same materials as that of the claimed invention, then using Atshshi's method of forming a hard etch mask comprising an insulating material over the first insulating layer, would inherently result in a selectivity between the first insulating layer and the hard etch mask that is greater than fifty to one.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hsue in view of Nulty by using Atsushi's method of forming a hard mask and selectively etching a contact hole through the hard mask an insulating layer for the purpose of improving the manufacture of a semiconductor device.

Hsue in view of Nulty and further in view of Atsushi differs in failing to teach the hard etch mask comprises silicon dioxide, **in claim 17**.

Ploessl teaches forming a TEOS (same as silicon dioxide) hard mask (column 3, lines 50 - 61).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hsue in view of Nulty and further in view of Atsushi by forming a hard etch mask comprising silicon dioxide as taught by Ploessl for the purpose of improving the method of making a semiconductor device.

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fitch (US 5,376,562) in view of Avanzino et al. (US 5,776,834).

Fitch teaches forming dielectric layer (same as applicant's undoped silicate glass) **20** over dielectric layer (same as applicant's doped silicon dioxide) **18** and the diffusion **14** (column 3, lines 35-42). The dielectrics may vary in physical and chemical composition based upon the function they perform and may be silicon dioxide, TEOS, BPSG, and or the like (column 3, lines 43-52).

Fitch further teaches the etching of the dielectric layers **16** and **20** and conductive layer **18** results in an opening that is self-aligned to the mask opening (column 4, lines 5-8 and 33-36; and Figures **1** and **2**), which reads on,

forming a hard mask comprising substantially undoped silicate glass over an insulating layer comprising doped silicon dioxide, the hard mask having opening over a contact hole location; and

forming a contact hole at the contact hole location through the insulating layer between conducting structures separated form one another and having sidewalls, without forming a protective liner over the conducting structures.

Fitch differs in failing to teach conducting structures separated form one another by less than 0.4 microns, **in claim 18.**

Avanzino teaches a pair of conductive lines having a gap of about 0.5 microns or less (Abstract), which reads on conducting structures that are separated from one another by less than 0.4 microns.

It would have been obvious to one having ordinary skill in the art to modify Fitch by using conductive lines that are less than 0.5 microns or less as taught by Avanzino for the purpose of improving the method of manufacturing a semiconductor device.

10. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fitch (562) in view of Avanzino ('834) as applied to claim 18 above, and further in view of Figura ('064).

Fitch in view of Avanzino differs in failing to specify a phosphorous doping concentration of greater than 5% by weight, **in claim 19**.

Figura teaches a silicon dioxide material, such as borophosphosilicate glass (BPSG) having phosphorus dopant of from 1 and 10%, which falls within the range of phosphorous dopant that is greater than 5% (column 3, lines 15-18).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Fitch in view of Avanzino by implanting silicon dioxide with a phosphorous dopant that is greater that 5% for the purpose of enhancing the conductive properties of an intrinsic insulative material such as SiO_2.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 703-306-9074. The examiner can normally be reached on Second Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703-308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703-972-9310 for regular communications and 703-972-9311 for After Final communications.

ltue
October 5, 2002